AMENDMENT TO THE SPECIFATION:

Please delete paragraph **[43]** and replace it with the following amended paragraph:

[43] One embodiment of the present invention uses an all-digital PLL to generate clock F1 from the clock C1. It should be appreciated that in one embodiment clock C1 has a higher speed than clock F1 for example, although other arrangements are contemplated. One process for generating the original or first clock frequencies from the higher speed clock C1 is illustrated in Figs. 7A and 7B. An overview of the process is illustrated in Fig. 7A, while a more detailed process is illustrated in Fig. 7B. in this embodiment, the operations are performed by the second order feedback look of an all-digital ~~PPL~~ PLL, for example.